REMARKS

This Amendment is submitted in answer to the Office Action dated July 20, 2009, having a shortened statutory period set to expire October 20, 2009.

I. Rejection under 35 U.S.C. § 103

At page 3 of the present Office Action, Claims 1-6 and 18-24 are rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,697,919 to *Gharachorloo et al.* (*Gharachorloo*) in view of U.S. Patent Publication No. 2003/0120881 to *Lai et al.* (*Lai*) and U.S. Patent No. 5,926,831 to *Revilla et al* (*Revilla*). That rejection is respectfully traversed, and favorable reconsideration of the claims is requested.

A. Combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the speculative memory access recited in exemplary independent Claim 1

The combination of *Gharachorloo*, *Lai* and *Revilla* does not render exemplary Claim 1 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose a memory controller that performs speculative memory access as recited in exemplary Claim 1 as amended:

> ... wherein said memory controller, responsive to receipt of a memory access request broadcast to the memory controller and the plurality of cache memories, said memory access request specifying a target system memory address:
>
> if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing said system memory; and
>
> if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

At indicated at pages 7-8 of the present Office Action, the combination of *Gharachorloo* and *Lai* discloses a page-table register unit that tracks addresses of previous memory access requests, and

if an address match occurs for a next memory access request, enables precharge of the memory during a current access to reduce access latency. See, e.g., *Lai*, paragraphs [0017] and [0029]. At pages 8-9 the Examiner then attempts to combine *Gharachorloo* and *Lai* with *Revilla* to obtain a memory controller having a memory speculation mechanism as claimed.

Applicant respectfully traverses the Examiner's conclusion of obviousness because the combination of *Gharachorloo*, *Lai* and *Revilla* would not cause an ordinarily skilled artisan to have arrived at the invention recited in exemplary Claim 1. In the rejection, the Examiner specifically relies upon col. 5, lines 35-37 and col. 6, lines 45-55 of *Revilla*, which disclose an arrangement in which a memory controller receives and services an access request (see, e.g., *Revilla*, Figure 2, block 58) and additionally conditionally performs additional speculative operation(s) only if a guard bit received from a processor in conjunction with the access request is not set (see, e.g., *Revilla*, Figure 2, block 64). Thus, the Examiner's combination of *Gharachorloo*, *Lai* and *Revilla* results in a system in which speculative precharging is performed during servicing of a current access request in response to address matching in a page-table register unit and in which additional speculative accesses can be performed if a guard bit supplied by the processor is not set.

However, the combination of *Gharachorloo*, *Lai* and *Revilla* fails to disclose a memory controller that, "responsive to receipt of a memory access request," "speculatively initiates access to the system memory to service the memory access request in advance of receipt by the memory controller of a coherency message indicating whether or not said memory access request is to be serviced by the memory controller accessing said system memory." In other words, the combination of cited references does not disclose performing speculative memory access for a current request after the memory request is received (i.e., "responsive to receipt of a memory access request"), but before a coherency message is received that confirms whether or not the memory controller is to service the memory access request (i.e., before performing the access to the system memory becomes non-speculative). The combination of references simply does not disclose any speculative memory access for a current memory access request, much less one governed by the timing constraints specified in exemplary Claim 1.

Further, as argued previously, the combination of cited references does not disclose or render obvious different timings of access to system memory relative to a coherency message based upon a memory speculation mechanism, as claimed. In other words, the combination of cited references does not disclose speculatively accessing system memory before a coherency message is received if the memory speculation mechanism indicates a speculative access and non-speculatively accessing system memory after a coherency message is received if the memory speculation mechanism indicates a non-speculative access. In fact, the combination of cited references does not disclose the claimed "coherency message" at all.

In view of the failure of the combination of cited references to disclose all features of exemplary Claim 1, Applicant respectfully submits that the rejection of exemplary Claim 1, similar Claims 9 and 14, and their respective dependent claims under 35 U.S.C. § 103 is overcome.

B. Combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in exemplary dependent Claim 3

The combination of *Gharachorloo*, *Lai* and *Revilla* also does not render exemplary Claim 3 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 3:

> … said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

At page 4 of the present Office Action, the Examiner again relies upon *Gharachorloo's* disclosure of a cache directory 180, instruction-level parallelism, simultaneous multithreading (SMT), and out-of-order execution as teaching the features of Claim 3. Applicant respectfully traverses the Examiner's position because none of these features of *Gharachorloo's* processor cores discloses a memory speculation table of a memory controller that stores a per-thread history, as required by the recitation that the "memory speculation table stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores." Because the combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in exemplary Claim 3, Applicant respectfully submits that the rejection of exemplary Claim 3 and

similar Claims 10 and 15 under 35 U.S.C. § 103 is overcome.

C. Combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in exemplary dependent Claim 4

The combination of *Gharachorloo*, *Lai* and *Revilla* also does not render exemplary Claim 4 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 4:

> … said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

At page 4 of the present Office Action, the Examiner relies, *inter alia*, upon *Gharachorloo's* disclosure of memory banks as teaching the features of Claim 4. Applicant respectfully traverses the Examiner's position because *Gharachorloo's* disclosure of memory banks does not disclose a memory speculation table of a memory controller that stores a per-bank history, as required by Claim 4. Further, *Lai* teaches that the access history relied upon by the Examiner is not stored on a per-bank basis, but rather for precise memory addresses. Because the combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in exemplary Claim 4, Applicant respectfully submits that the rejection of exemplary Claim 4 and similar Claims 11 and 16 under 35 U.S.C. § 103 is overcome.

D. Combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in exemplary dependent Claim 5

The combination of *Gharachorloo* and *Lai* also does not render exemplary Claim 5 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 5:

> … wherein said coherency message comprises a combined response representing a systemwide response to said memory access request.

At page 5 of the present Office Action, the Examiner relies upon *Gharachorloo's* column 23, lines 14-60, which disclose various updates to a coherency state field in a coherence directory.

Applicant respectfully traverses the Examiner's position because the cited passage of *Gharachorloo* nowhere discloses a coherency message (of Claim 1) that is a combined response for a memory access request, as recited in Claim 5. Because the combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in exemplary Claim 5, Applicant respectfully submits that the rejection of exemplary Claim 5 and similar Claim 17 under 35 U.S.C. § 103 is overcome.

E. Combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in exemplary dependent Claim 6

The combination of *Gharachorloo* and *Lai* also does not render exemplary Claim 6 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features of Claim 6:

> … said memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller.

At page 5 of the present Office Action, the Examiner again relies upon *Gharachorloo's* column 21, lines 59-63 as disclosing that *Gharachorloo's* cache coherence protocol enables sharing of memory lines across multiple nodes. Applicant respectfully traverses the Examiner's position because *Gharachorloo's* disclosure of a cache coherency protocol fails to disclose the speculative initiation of access to a system memory by a first system memory controller based upon historical information recorded by a second memory controller, as recited by Claim 6. Because the combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in exemplary Claim 6, Applicant respectfully submits that the rejection of exemplary Claim 6 and similar Claims 13 and 18 under 35 U.S.C. § 103 is overcome.

F. Combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in Claim 19

The combination of *Gharachorloo*, *Lai* and *Revilla* also does not render Claim 19 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features recited therein:

> … wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of

speculative access to the system memory as indicated by the coherency message.

With reference to these features, page 9 of the present Office Action cites again col. 5, lines 35-60 of *Revilla*, which disclose an arrangement in which a memory controller receives and services an access request (see, e.g., *Revilla*, Figure 2, block 58) and additionally conditionally performs additional speculative operation(s) only if a guard bit received from a processor in conjunction with the access request is not set (see, e.g., *Revilla*, Figure 2, block 64). The cited passage does not disclose an update to a memory speculation mechanism in response to confirmation of correctness of speculative access to system memory as claimed. Consequently, the combination of *Gharachorloo*, *Lai* and *Revilla* does not render exemplary Claim 19 and similar Claims 21 and 23 unpatentable under 35 U.S.C. § 103.

G. Combination of *Gharachorloo*, *Lai* and *Revilla* does not disclose the features recited in Claim 20

The combination of *Gharachorloo*, *Lai* and *Revilla* also does not render Claim 20 unpatentable under 35 U.S.C. § 103 because that combination of references does not disclose the following features recited therein:

> … wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

With reference to these features, page 9 of the present Office Action cites again col. 5, lines 35-60 of *Revilla*, which are described above. The cited passage does not disclose discarding data associated with a memory access request responsive to a coherency message indicating speculative access to system was incorrect as claimed. Consequently, the combination of *Gharachorloo*, *Lai* and *Revilla* does not render exemplary Claim 20 and similar Claims 22 and 4 unpatentable under 35 U.S.C. § 103.

II. CONCLUSION

Having now addressed and overcome each outstanding rejection, Applicant respectfully submits that all claims now pending are in condition for allowance and respectfully requests such allowance.

Please charge any fee necessary to further the prosecution of this application to IBM Corporation Deposit Account No. **09-0447**.

Respectfully submitted,

/Brian F. Russell/

Brian F. Russell
Reg. No. 40,796
DILLON & YUDELL LLP
8911 N. Capital of Texas Hwy., Ste. 2110
Austin, Texas 78759
(512) 343-6116

ATTORNEY FOR APPLICANT(S)